Notice of Allowability	Application No.	Applicant(s)	
	09/939,277	GARNETT ET AL.	
	Examiner	Art Unit	
	Hong C. Kim	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on 3/7/05*.

2. ☒ The allowed claim(s) is/are *1 2 27 3-6 23-26 28 29 7-11 22 12-21 which are renumbered to 1-29*.

3. ☒ The drawings filed on *07 March 2005* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 3/7/05
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Detailed Action

1. Claims 1-29 are presented for examination. This office action is in response to the amendment filed on 3/7/2005.

2. The information disclosure statement (IDS) submitted on 3/7/2005 is being considered by the examiner.

REASONS for ALLOWANCE

3. The following is an Examiner's statement of reasons for the indication of allowable subject matter: renumbered claims 1-29 are allowable over the prior art of record because the arguments set forth in the amendment filed on 3/7/2005 are persuasive. The claims are allowable over the prior art of record because the claims are distinguished from the prior art of record for the reasons as set forth in the amendment filed on 3/7/2005 and because an update of a search previously made does not detect the combined claimed elements as set forth in the claims 1-29. Specifically, claims are allowable over the prior art of record because none of the prior art of record teaches or fairly suggests a bridge includes a direct memory access controller that is operable to respond to an error state by controlling the copying of dirtied blocks of a main memory of the first processing set indicated in a dirty memory of the first processing set to the main memory of another processing set as described in the specification and together with combination of other claimed element as set forth in the claims. Also the reasons for allowance of the claims over the prior art of record is

believed to be clear from the prosecution records taken as a whole. Therefore, claims 1-29 are allowable over the prior art of records.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably **accompany** the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons For Allowance."

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong C Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
(703) 872-9306

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

HK
Primary Patent Examiner
May 17, 2005

IN THE CLAIMS:

1. (currently amended) A computer system comprising:

at least two processing sets, each processing set including a main memory; and

a bridge connecting the processing sets,

wherein at least a first processing set further includes a dirty memory having dirty indicators for indicating dirtied blocks of the main memory of the first processing set, and

wherein the bridge includes a direct memory access controller that is operable to respond to ~~a fault~~ an error state by controlling the copying of the dirtied blocks of the main memory of the first processing set indicated in the dirty memory of the first processing set to the main memory of another processing set.

2. (original) The computer system of claim 1, wherein the direct memory access controller is operable to search the dirty memory for dirty indicators indicative of dirtied blocks.

4 ~~3~~. (original) The computer system of claim 1, wherein the dirty memory comprises control logic operable to search the dirty memory for dirty indicators indicative of dirtied blocks.

4

5 ~~4~~. (original) The computer system of claim ~~3~~, wherein the control logic is operable to output references to the dirtied blocks of the main memory to be copied.

5

6. ~~5~~. (original) The computer system of claim ~~4~~, wherein the control logic is operable to buffer references to the dirtied blocks of the main memory to be copied.

5

7 ~~6~~. (original) The computer system of claim ~~4~~, wherein the references to the dirtied blocks comprises addresses for the dirtied blocks.

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~~7~~. (original) The computer system of claim 1, wherein a block of main memory is a page of main memory.

15

8. (original) The computer system of claim 1, wherein each dirty indicator comprises a single bit.

16

9. (original) The computer system of claim 1, wherein the direct memory access controller is operable to instigate a search of the dirty memory for dirty indicators indicative of dirtied blocks.

17

10. (original) The computer system of claim 1, wherein each processing set includes a dirty memory.

18

11. (original) The computer system of claim 1, wherein the processing sets are operable in lockstep, the computer system comprising logic operable to attempt to reinstate an equivalent memory state in the main memory of each of the processor following a lockstep error.

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12. (currently amended) A method for reintegrating the main memory of a computer system comprising:

at least two processing sets, each processing set including a main memory; and

a bridge connecting the processing sets,

the method comprising:

recording an indicator of a block of the main memory of a first processing set that has been dirtied in a dirty memory in the first processing set; and

a direct memory access controller in the bridge responding to ~~a fault~~ an error state by controlling the copying of dirtied blocks of the main memory of the first processing set indicated in the dirty memory of the first processing set to the main memory of another processing set.

21 20

13. (original) The method of claim 12, wherein the direct memory access controller searches the dirty memory for dirty indicators indicative of dirtied blocks.

22 20
~~14~~. (original) The method of claim ~~12~~, wherein dirty memory control logic searches the dirty memory for dirty indicators indicative of dirtied blocks.

23 22
~~15~~. (original) The method of claim ~~14~~, wherein the control logic outputs references to the dirtied blocks of the main memory to be copied.

24 23
~~16~~. (original) The method of claim ~~15~~, wherein the control logic buffers references to the dirtied blocks of the main memory to be copied.

25 23
~~17~~. (original) The method of claim ~~15~~, wherein the references to the dirtied blocks comprises addresses for the dirtied blocks.

26 20
~~18~~. (original) The method of claim ~~12~~, wherein a block of main memory is a page of main memory.

27 20
~~19~~. (original) The method of claim ~~12~~, wherein each dirty indicator comprises a single bit.

28 20
~~20~~. (original) The method of claim ~~12~~, wherein the direct memory access controller instigates a search of the dirty memory for dirty indicators indicative of dirtied blocks.

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~~21~~. (original) The method of claim ~~12~~, wherein the processing sets are operable in lockstep, the method comprising attempting to reinstate an equivalent memory state in the main memory of each of the processor following a lockstep error.

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~~22~~. (new) The computer system of claim 1, wherein the error state is due to a lockstep error, wherein said direct memory access controller controlling the copying of the dirtied blocks of the main memory of the first processing set to the main memory of another processing set is part of a reintegration process to reinstate an equivalent memory state in the main memory of each of the processing sets following the lockstep error.

8 4
23. (new) The computer system of claim 3, wherein each processing set further comprises a buffer, wherein the control logic is operable to store in the buffer addresses of the dirtied blocks of the main memory to be copied, wherein during a reintegration process the direct memory access controller is operable to access the buffer to determine whether any blocks of the main memory of the first processing set are dirtied.

9 24. (new) The computer system of claim 23, wherein the first processing set further comprises a counter that is operable to indicate a number of addresses corresponding to the dirtied blocks to be copied, wherein the number is incremented by the control logic each time an address is added to the buffer, and the number is decremented by the direct memory access controller each time the direct memory access controller copies a dirtied block of the main memory in the first processing set to the another processing set.

10 25. (new) The computer system of claim 23, wherein the buffer comprises a start pointer and an end pointer, wherein the start and end pointers encompass a portion of the buffer containing addresses of the dirtied blocks of the main memory to be copied.

11 4
26. (new) The computer system of claim 3, wherein the control logic is operable to directly provide the direct memory access controller addresses of the dirtied blocks of the main memory to be copied.

3
27. (new) The computer system of claim 2, wherein the direct memory access controller comprises a counter that is operable to count a number of dirtied blocks found in the main memory of the first processing set.

12 4
28. (new) The computer system of claim 3, wherein the dirty indicators being stored in groups with each group having associated therewith a parity indicator computed from the dirty indicator values of the group, wherein the control logic being operable on reading the dirty indicators of a group and a corresponding parity indicator to calculate a parity indicator value based on the dirty indicator values read for the group to determine an integrity of the group, wherein the control logic is configured to identify all dirty

indicators of the group as representing a dirtied state where the calculated parity indicator value is different from the parity indicator value read for that group.

13 4
~~29~~. (new) The computer system of claim ~~3~~, wherein the dirty memory comprising:

a lower level memory operable to store groups of dirty indicators, wherein each dirty indicator being associated with a respective block of main memory and being settable to a predetermined state to indicate that the block of main memory associated therewith has been dirtied;

at least one higher level memory operable to store groups of dirty group indicators, wherein each dirty group indicator being settable to a given state indicative that a group of dirty indicators of the lower level memory has at least one dirty indicator in the predetermined state indicative that a block of main memory associated therewith has been dirtied;

wherein the control logic is operable to read a dirty group indicator from the higher level memory and to treat the group of dirty indicators associated therewith as dirtied in response to the dirty group indicator having the given state; and

wherein, in response to the dirty group indicator having the given state, for each dirty indicator in the group of dirty indicators, the control logic is operable to read the dirty indicator from the lower level memory and to treat the block of main memory associated therewith as dirtied in response to the dirty indicator having the predetermined state.